Abstract of the Disclosure

A memory device includes at least two cell blocks connected to a global bit line for outputting data in response to an instruction; at least one global bit line connection unit for selectively connecting the global bit line to each cell block under control of a control block, one global bit line connection unit being allocated between the two cell blocks; and said control block for controlling output of data stored in each cell block to the global bit line and restoration of the outputted data of the global bit line to the original cell block or another cell block which is determined by depending upon whether data in response to a next instruction is outputted from the original cell block or another cell block.